In the Specification:

Please substitute the following paragraph for the corresponding (previously amended) paragraph beginning at the indicated location in the specification as originally filed.

Page 6, line 15+:

The instruction registering stage 4 includes a ~~ROB registration order~~ <u>reorder</u> buffer (ROB) 21, an operation instruction buffer 22, and a memory access instruction buffer 23. the ROB 21 is connected to the instruction decoders 15 through ~~decode register~~ 18 of the instruction decoding stage 3. The ROB 21 sequentially registers all instructions in order of input and sequentially releases them in order of completion. The ROB 21 stores the order of instructions and is used to detect the dependence of on each other and to confirm the completion of instructions. The operation instructions are registered at the operation instruction buffer 22 and then issued, as will be described specifically later. The memory access instructions are registered at the memory access instruction buffer 23 and then issued, as will also be described specifically later.